DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Winter Examination – 2022

Course: B. Tech. **Branch: E&TC** **Semester: VII**

Subject Code & Name: BTEXPE703C CMOS Design

Max Marks: 60 **Date: 01/02/2023** **Duration: 3 Hours**

Instructions to the Students:

1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

		(Level/CO)	Marks
Q. 1	**Solve Any Two of the following.**		**12**
A)	Draw and explain transfer characteristics of CMOS inverter.	**1**	**6**
B)	Implement $Y = (A.B + \bar{C}.D) + F$ function using static CMOS design.	**2**	**6**
C)	Draw the schematic and layout for two input CMOS NOR gate, Use CMOS Lambda based design rules.	**2**	**6**
Q.2	**Solve Any Two of the following.**		**12**
A)	Explain various steps involved in CMOS inverter n-well fabrication	**1**	**6**
B)	Explain leakage power in CMOS inverter. What are ways to reduce it?	**1**	**6**
C)	Implement 4:1 multiplexer using CMOS transmission gates.	**2**	**6**
Q. 3	**Solve Any Two of the following.**		**12**
A)	Explain Channel length Modulation the non-ideal effect in MOSFET's.	**1**	**6**
B)	Write electrical, logical effort, parasitic effort for four input NOR gate.	**2**	**6**
C)	Explain CMOS λ-based design rules in detail.	**1**	**6**
Q.4	**Solve Any Two of the following.**		**12**
A)	Implement JK Flip-Flop using Static CMOS design style.	**2**	**6**
B)	Implement $Y = \overline{ABC}$ using dynamic CMOS design style.	**2**	**6**
C)	Explain all the parasitic capacitances of the MOSFET in detail	**1**	**6**
Q. 5	**Solve Any Two of the following.**		**12**
A)	Explain DIBL and subthreshold leakage for MOSFET	**1**	**6**
B)	Implement half adder combinational circuit using static CMOS logic.	**2**	**6**
C)	Implement two input CMOS AND/NAND gate using Dual rail Dominologic	**2**	**6**

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