DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Regular & Supplementary Winter Examination-2023

Course: B. Tech. **Branch: Electronics Engineering** **Semester: VII**

Subject Code & Name: BTEXPE702E CMOS Design

Max Marks: 60 **Date: 4/1/2024** **Duration: 2:00 to 5:00 PM**

Instructions to the Students:

1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Use graph paper with proper scale for drawing layout.*

		(CO)	Marks
Q.1	**What do you mean by Photolithography? draw neat diagrams and explain CMOS n-well fabrication process in detail.**	**4**	**12**
Q.2	**Draw schematic & stick diagram for two input CMOS OR gate with equal rise and fall time.**	**2**	**4**
	Draw Layout for two input static CMOS OR gate (on graph paper with proper scale)	**1**	**8**
Q. 3	**Solve Any Two of the following.**		
A)	**What is Elmore delay model? What is the effect of interconnect on parasitic on delay?**	**2**	**6**
B)	**Implement logic function $Y = A\overline{B}(C + \overline{D})$ using Static CMOS logic**	**1**	**6**
C)	**Explain static and dynamic power in CMOS circuits. What is an activity factor?**	**2**	**6**
Q.4	**Solve Any Two of the following.**		
A)	**Implement half adder circuit using static CMOS logic**	**2**	**6**
B)	**Write electrical, logical effort, parasitic effort for four input NOR gate.**	**2**	**6**
C)	**Draw 6T SRAM cell and explain its working in detail**	**3**	**6**
Q. 5	**Solve Any Two of the following.**		
A)	**A combinational circuit is defined by following functions**	**1**	**6**

$$F_1(A, B, C) = \sum m(1, 3, 6, 7)$$

$$F_2(A, B, C) = \sum m(0, 2, 4, 5)$$

Implement both functions using a PLA

B)	**Draw and explain the Voltage Transfer Characteristics for CMOS inverter in detail.**	**4**	**6**
C)	**Write a short note on CMOS scaling**	**2**	**6**

***** End *****