DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Supplementary Winter Examination – 2023

Course: B. Tech. Branch: E&TC Engineering/Electronics Semester: VII

Subject Code & Name: BTEXPE703C CMOS Design

Max Marks: 60 Date: 6/1/2024 Duration: 2:00 to 5:00 PM

Instructions to the Students:

1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in () in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

		(CO)	Marks
Q. 1	**Solve Any Two of the following.**		**12**
A)	**Draw and explain transfer characteristics of CMOS inverter.**	**1**	**6**
B)	**Implement $Y = (A + B).CD$ function using static CMOS design style.**	**2**	**6**
C)	**Draw the schematic and layout for three input CMOS NOR gate, Use CMOS Lambda based design rules.**	**2**	**6**
Q.2	**Solve Any Two of the following.**		**12**
A)	**Write a short note on CMOS scaling**	**1**	**6**
B)	**Explain leakage power in CMOS inverter. What are ways to reduce it?**	**1**	**6**
C)	**Implement 4:1 multiplexer using CMOS transmission gates.**	**2**	**6**
Q. 3	**Solve Any Two of the following.**		**12**
A)	**What are various Short Channel Effects? How to avoid them?**	**1**	**6**
B)	**Write electrical, logical effort, parasitic effort for four input NOR gate.**	**2**	**6**
C)	**Explain CMOS λ-based design rules in detail.**	**1**	**6**
Q.4	**Solve Any Two of the following.**		**12**
A)	**Implement JK Flip-Flop using Static CMOS design style.**	**2**	**6**
B)	**Explain dynamic CMOS logic. Compare it with static CMOS logic**	**2**	**6**
C)	**Explain all the parasitic capacitances of the MOSFET in detail**	**1**	**6**
Q. 5	**Solve Any Two of the following.**		**12**
A)	**Implement 2-bit magnitude comparator using static CMOS logic**	**1**	**6**
B)	**Implement half adder combinational circuit using static CMOS logic.**	**2**	**6**
C)	**Implement two input CMOS AND/NAND gate using Dual rail Domino logic**	**2**	**6**

***** End *****