DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Winter End Semester Examination – March 2023

Course: B. Tech. **Semester: III**

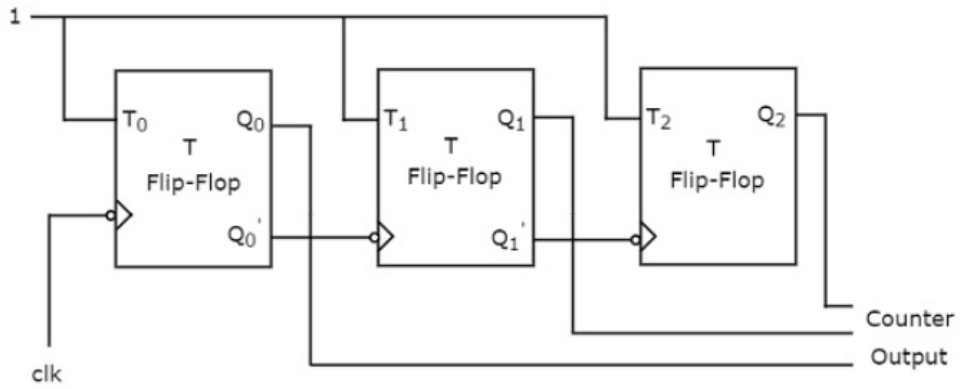
Subject Code & Name: BTETC303 & Digital Electronics

Max Marks: 60 **Date:13/03/2023** **Duration: 3 Hr.**

Instructions to the Students:

1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

		(Level/CO)	Marks
Q. 1	**Solve Any Two of the following.**		**12**
A)	Convert the following Boolean equation into standard SOP and POS form. F(A,B,C) = AB + AC' + BC	**L2**	**6**
B)	Write VHDL code for full adder using Structural architecture method.	**L3**	**6**
C)	Explain TTL logic in detail.	**L2**	**6**
Q.2	**Solve Any Two of the following.**		**12**
A)	Draw the counter output of the following sequential circuit using clock diagram.	**L2**	**6**

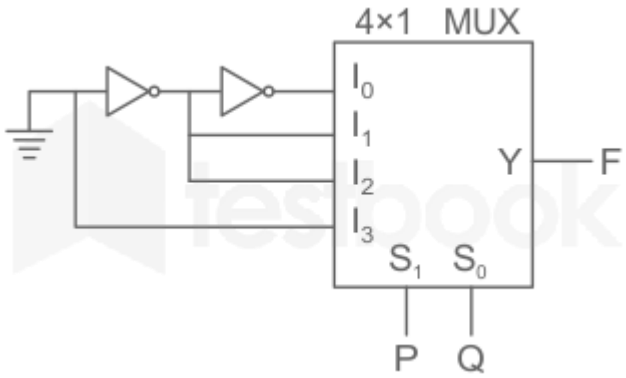


B)	What is the difference between TTL and CMOS and ECL?	**L2**	**6**
C)	Explain General Architecture of CPLD in detail.	**L2**	**6**
Q. 3	**Solve Any Two of the following.**		**12**
A)	Draw the Moore state diagram for One bit Serial adder.	**L2**	**6**
B)	Implement the following Boolean functions using PAL and PROM. $A(X,Y,Z)=\sum m(4,6,7)$, $B(X,Y,Z)=\sum m(2, 4, 5,6)$	**L3**	**6**

C)	Minimise the following function in SOP and POS form using K-Maps: F(A, B, C, D) = m(1, 2, 6, 7, 8, 13, 14, 15) + d(0, 3, 5, 12)	**L3**	**6**

Q.4 Solve Any Two of the following. **12**

A)	Explain the universal shift register operation with diagram.	**L3**	**6**
B)	The logic function is implemented by the multiplexer circuit is ("ground implies a logic 0") find the output of F?	**L3**	**6**



C)	Write VHDL code for 4-bit up counter.	**L3**	**6**

Q. 5 Solve Any Two of the following. **12**

A)	Implement the following function using i) multiplexer 8x1 ii) multiplexer 2x1 F(A,B,C,D) = m(0,1,3,5,7,10,11,14)	**L3**	**6**
B)	Design sequence detector to detect three or more consecutive 1's in string of bits coming through an input lines.	**L3**	**6**
C)	i) What is disadvantage in SR flipflop? ii) What is difference between T flipflop and D flipflop? iii) Write down the next state equation of T flipflop.	**L2**	**6**

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