DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Regular & Supplementary Winter Examination-2023

Course: B. Tech. **Branch :Electronics Engineering** **Semester : V**

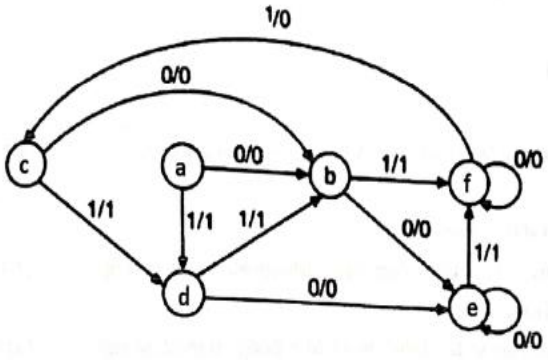
Subject Code & Name: **(BTEXOE505A) Digital System Design**

Max Marks: 60 **Date:10-01-24** **Duration: 3 Hr.**

Instructions to the Students:

1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

		(Level/CO)	Marks
Q. 1	**Solve Any Two of the following.**		**12**
A)	Explain the following data objects with syntax in VHDL File, signal, Variable, file.	**CO4**	**6**
B)	Explain the various data types in VHDL.	**CO4**	**6**
C)	Write different types of delays used in VHDL.	**CO4**	**6**
Q.2	**Solve Any Two of the following.**		**12**
A)	What is subprogram? Explain 'Function' and 'Procedure' with their syntax.	**CO4**	**6**
B)	What is the purpose of test bench in VHDL? Design Half Adder and write test bench code.	**CO1, CO4**	**6**
C)	Describe the concepts of component declaration and instantiation with suitable example.	**CO1, CO4**	**6**
Q. 3	**Solve Any Two of the following.**		**12**
A)	Design half-subtractor and Write a VHDL code using behavioral modeling.	**CO1**	**6**
B)	Design 3:8 decoder and write VHDL code using structural modeling.	**CO2**	**6**
C)	Design a full-adder using two half-adders and write VHDL code for it.	**CO1**	**6**
Q.4	**Solve Any Two of the following.**		**12**
A)	Define FSM. Also Differentiate between Mealy and Moore machines.	**CO3**	**6**
B)	Reduce the following state diagram and prepare a state table for reduced state diagram.	**CO3**	**6**



C)	Draw the Melay state diagram for sequence detector 1001 and 0110.	**CO3**	**6**

Q. 5 Solve Any Two of the following. **12**

A)	Explain the following terms in details i. Clock skew ii. Dynamic Hazards iii. PLD	**CO3**	**6**
B)	Explain Metastability and Synchronizers.	**CO3**	**6**
C)	Briefly explain the architecture of a Complex Programmable Logic Device	**CO4**	**6**

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