

Course: B. Tech.

Branch : Electronics Engineering

Semester :V

Subject Code & Name: [BTEXOE505A] Digital System Design

Max Marks: 60

Date:14/02/2023

Duration: 3 Hours

Instructions to the Students:

1. All the questions are compulsory.
2. The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in () in front of the question.
3. Use of non-programmable scientific calculators is allowed.
4. Assume suitable data wherever necessary and mention it clearly.

	(CO)	Marks
Q. 1 Solve Any Two of the following.		12
A) Explain any four data objects in VHDL with syntax.	CO1	6
B) Explain Design flow for Digital System Design using VHDL.	CO1	6
C) Explain the following sequential statements with Syntax: if statement next exit return loop case	CO2	6
Q.2 Solve Any Two of the following.		12
A) What is test bench in VHDL and write test bench code for 4:1 MUX.	CO2	6
B) Explain attributes in VHDL with example.	CO2	6
C) Write a short note on configuration.	CO2	6
Q. 3 Solve Any Two of the following.		12
A) Design Octal to Binary Encoder and write VHDL code.	CO1	6
B) Design full subtractor and write VHDL code using dataflow modeling.	CO1	6
C) Design 8 to 1 Multiplexer and write its VHDL code.	CO1	6

Q.4 Solve Any Two of the following.

12

- A) What is a state assignment in Finite State Machine? Draw the state diagram from the following state table.**

CO2

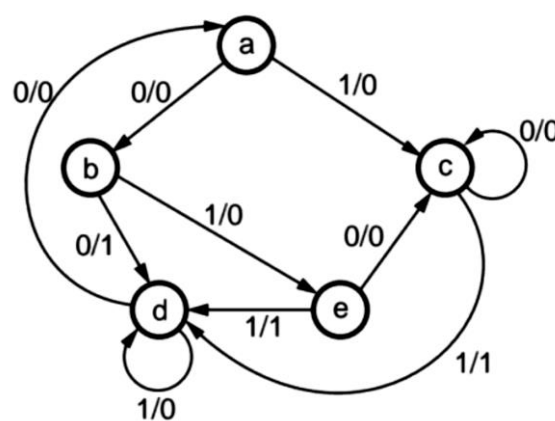
6

Present state	Input x=0		Input x=1	
	Next state	Output	Next state	Output
q1	q1	0	q2	0
q2	q2	1	q3	0
q3	q2	0	q3	1

- B) Reduce the following State diagram and prepare a State table for the reduced State diagram**

CO2

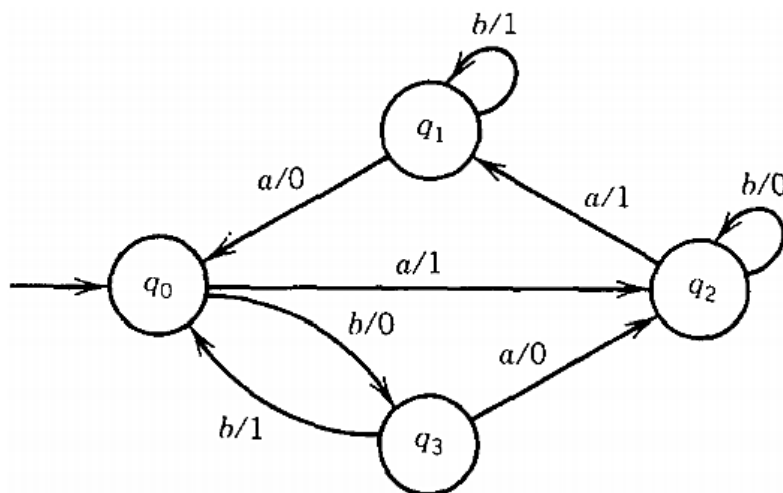
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- C) Convert Mealy machine to Moore machine from the following diagram.**

CO2

6



Q. 5 Solve Any Two of the following.

12

- A) Write a short note on place & route process.**
B) Write a short note on ROM.
C) Write a short note on Programmable Logic Array (PLA).

CO2

6

CO2

6

CO2

6

***** End *****