DR. BABASAHEB AMBEDKAR TECHNOLOGICAL UNIVERSITY, LONERE

Supplementary Summer-2023

Course: B. Tech. **Branch :Electronics Engineering** **Semester : V**

Subject Code & Name: Digital System Design (BTEXOE505A)

Max Marks: 60 **Date:19/08/2023** **Duration: 3 Hr.**

Instructions to the Students:

1. *All the questions are compulsory.*
2. *The level of question/expected answer as per OBE or the Course Outcome (CO) on which the question is based is mentioned in ( ) in front of the question.*
3. *Use of non-programmable scientific calculators is allowed.*
4. *Assume suitable data wherever necessary and mention it clearly.*

		(Level/CO)	Marks
Q. 1	**Solve/Answer Any Two of the following.**		**12**
A)	What is VHDL? And what are its key features for hardware description?	**CO1**	**6**
B)	Compare i)concurrent and sequential statements in VHDL ii) Data objects and signal drivers in VHDL,	**CO1,CO2**	**6**
C)	Design an 8-to-1 multiplexer using combinational logic and write its VHDL code.	**CO1,CO2**	**6**
Q.2	**Solve/Answer Any Two of the following.**		**12**
A)	Explain Read-Only Memory (ROM), Programmable Logic Array (PLA), and Programmable Array Logic (PAL) devices	**CO3**	**6**
B)	Design a 4-bit adder circuit using basic logic gates (AND, OR, XOR, etc.) and write VHDL code.	**CO1,CO2**	**6**
C)	Design 4-bit SISO shift register and write VHDL code	**CO3**	**6**
Q. 3	**Solve/Answer Any Two of the following.**		**12**
A)	Explain the various data types in VHDL.	**CO4**	**6**
B)	Explain different modeling styles of VHDL with suitable examples	**CO1**	**6**
C)	Write a VHDL entity and Architecture for the following function. $F(x) = (a + b)(c + d)$. Also draw the relevant logic diagram.	**CO2,CO4**	**6**
Q.4	**Solve/Answer Any Two of the following.**		**12**
A)	Explain about Simulation and Synthesis processes in VHDL.	**CO4**	**6**
B)	Write a VHDL program for a 2 bit Magnitude Comparator using Data Flow model.	**CO2,CO3**	**6**
C)	What is VHDL ? And Explain the following with syntax in VHDL File, signal , Variable	**CO4**	**6**
Q. 5	**Solve/Answer Any Two of the following.**		**12**
A)	Briefly explain the architecture of a Complex Programmable Logic Device	**CO4**	**6**
B)	Define FSM. Also Differentiate between Mealy and Moore machines in terms of their output generation and transition behavior	**CO3**	**6**
C)	Design 3:8 decoder and write VHDL code using structural modeling	**CO1,CO2**	**6**

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